

UTILITY SERIAL NUMBER	PATENT DATE	PATENT NUMBER
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SERIAL NUMBER 08/965,286	FILING DATE 11/06/97 RULE 60	CLASS <del>438</del> 251	SUBCLASS 553 565	GROUP ART UNIT 1987 2815	EXAMINER NADAN
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\*\*CONTINUING DATA\*\*\*\*\*  
 VERIFIED THIS APPLN IS A DIV OF 08/762,779 12/10/96, Now US. Patent  
 O.N. 5,976,940

\*\*FOREIGN APPLICATIONS\*\*\*\*\*  
 VERIFIED JAPAN P07-322962 12/12/95  
 O.N.



Foreign priority claimed 35 USC 119 conditions met	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	AS FILED →	STATE OR COUNTRY JPX	SHEETS DRAWGS. 24	TOTAL CLAIMS 10	INDEP. CLAIMS 3	FILING FEE RECEIVED \$790.00	ATTORNEY'S DOCKET NO. P97.2608
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TITLE BIPOLAR TRANSISTOR AND METHOD OF MAKING THE SAME SEMICONDUCTOR DEVICE  
 INCLUDING HIGH SPEED TRANSISTORS AND HIGH VOLTAGE TRANSISTORS  
 DISPOSED ON A SINGLE SUBSTRATE

U.S. DEPT. OF COMM./ PAT. & TM—PTO-436L (Rev.12-94)

PARTS OF APPLICATION FILED SEPARATELY		Applications Examiner	
NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
		Print Fig.	
Label Area		ISSUE BATCH NUMBER	
		PREPARED FOR ISSUE	
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Form PTO-436A  
 (Rev. 8/92)  
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